Q-8

LOAD-LINE ANALYSIS IN THE FREQUENCY DOMAIN WITH DISTRIBUTED AMPLIFIER DESIGN EXAMPLES

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ABSTRACT

Time-Domain analysis of a multi-FET circuit over a wide frequency range and for several power levels using SPICE is not practical because of excessive computer time causing high cost and slow feedback to the designer. The load-line analysis to be described is a linear technique in the frequency domain and is therefore fast. A load-line ellipse is generated at each node of interest and graphically displayed and superimposed on the I-V curves of the device at that node. The driving signal to the amplifier and the amplifier matching networks are adjusted so that the load-line ellipse just fills the linear region of the FET I-V characteristics. Amplifier designs based on this approach agree with measured results within 0.5 dB at frequencies up to 18 GHz. What allows this technique to give accurate results is the sampling of the branch current "inside" the FET model while the FET parasitics are absorbed into the rest of the amplifier circuit.

INTRODUCTION

A direct way for a designer to assess whether he has achieved optimum performance from a power FET is whether or not the FET is able to fully drive the load impedance both in voltage and current within the operating area of the FET I-V characteristics. If the device swings the load current from the V_{sat}-I_{DSS} point to just within the breakdown voltage near pinchoff, then the device has ranged over what is called here the "power triangle", and all the power handling capability of the device has been utilized. The application of a load-line technique at microwave frequencies yields a readily interpreted graphical display of whether the load line a device "sees" fills the power triangle; however, a method of comparison between the d-c I-V characteristics and the r-f operation which is affected by parasitics is needed if accurate results are to be obtained.

THE RF MODEL USED IN COMPARISON WITH DC CHARACTERISTICS

Figure 1 shows the d-c and r-f partitioning of the standard FET model. The model elements that account for the d-c I-V curves are shown in solid lines. Elements important at rf such as C_{gs} and C_{dg} are shown in dashed lines. R_{ds} as found by backfitting the model to measured S-parameters is included with the microwave parasitics, and the loading of R_{ds} on the drain I-V characteristics is removed. The common link that remains between the d-c and r-f models is the voltage-controlled current generator and the drain voltage. At lower frequencies, such as what is displayed on a 60-cycle curve tracer, the drain-terminal current is the same as that of the voltage-controlled current generator inside the FET model, but at microwave frequencies the voltage-controlled current generator produces what would be the drain-terminal current were it not for the r-f parasitics illustrated as dashed lines in Figure 1. The current generator rather than the drain-terminal current therefore provides the common link between the d-c operation and r-f operation. The r-f load line the device sees is therefore the locus of current-generator, drain-voltage coordinate pairs, and not that due to the combination of the drain-terminal current and drain voltage. As a result, the parasitic capacitances introduce a phase difference between the drain voltage and the voltage-controlled current generator causing the r-f load line to become an ellipse. This is shown in dashed lines superimposed on the I-V curves in Figure 2.

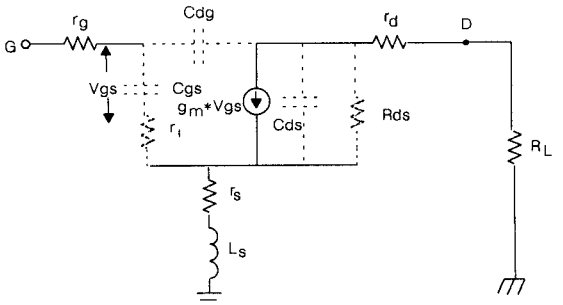

Figure 1. D-C and R-F Partitioning of the Standard FET Model. D-C elements are shown in solid lines, and r-f elements are shown in dashed lines.

LOAD-LINE CALCULATION

The basic technique is to compute by Y-matrix analysis the node voltages of the network,

$$[\bar{V}]_{nodes} = [\bar{Y}]^{-1}\,[\bar{I}]_{sources}\ .$$

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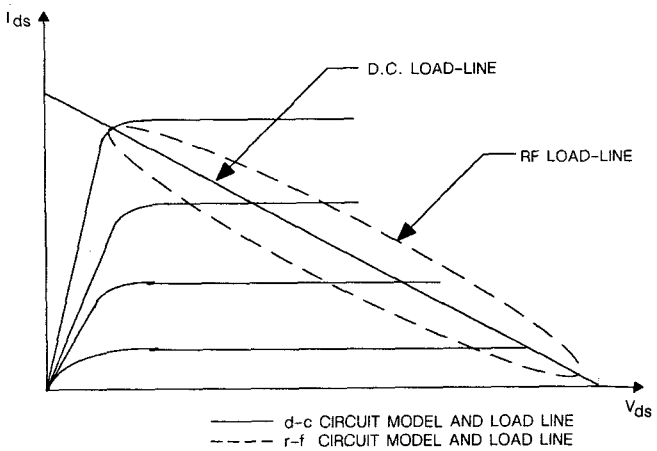

Figure 2. The R-F Load Line Becomes an Ellipse Because of the R-F Parasitics. G_m is assumed to be linear, but this assumption leads to less than 0.5 dB error.

$\bar{V}_1$, $\bar{V}'$, and $\bar{V}''$ of Figure 3 are obtained, for example, as a straight-forward result of the nodal analysis for a given value of $\bar{I}_{source} = I_{pk}\angle 0$. $\bar{I}_1$ is computed as $g_m(\bar{V}' - \bar{V}'')$. The load-line ellipse is then computed as a locus of $(\bar{I}_1, \bar{V}_1)$ pairs by taking real parts,

$$\mathrm{Re}\{I_{1pk}\angle\theta,\ V_{1pk}\angle\phi\} \ .$$

The ellipse is generated by stepping θ and ϕ in five-degree increments while keeping I_{1pk}, V_{1pk}, and $(\theta - \phi)$ constant. Since the nodal analysis is based on a-c, incremental modeling of the FETs and the rest of the network, the values for the d-c quiescent point are added to the (I_1, V_1) pairs, and when these pairs are superimposed on the FET I-V curves ellipses as in Figure 4 result.

DISTRIBUTED AMPLIFIER DESIGN EXAMPLES

1 X 4 DA

The usefulness of the technique is shown in the analysis of two types of 4-section distributed amplifiers (DA's). The conventional DA has one gate line and one drain line with the FETs spaced at uniform intervals, and is designated here as a 1 X 4 DA. A second kind of DA which was used to illustrate the technique has two gate lines and a common drain line and is designated as a 2 X 4 DA. The load lines of a 1 X 4 DA are shown in Figure 4. The load lines of FETs 1 through 4 are superimposed on the device I-V characteristics. Note FET #1 nearest the drain line termination is near vertical indicating a near short (backward wave voltage near zero), and that as the FETs are taken in order approaching the load, the load lines become progressively higher resistance, but not nearly as optimum as desired. The basic problem in designing a DA is that the characteristic impedance of

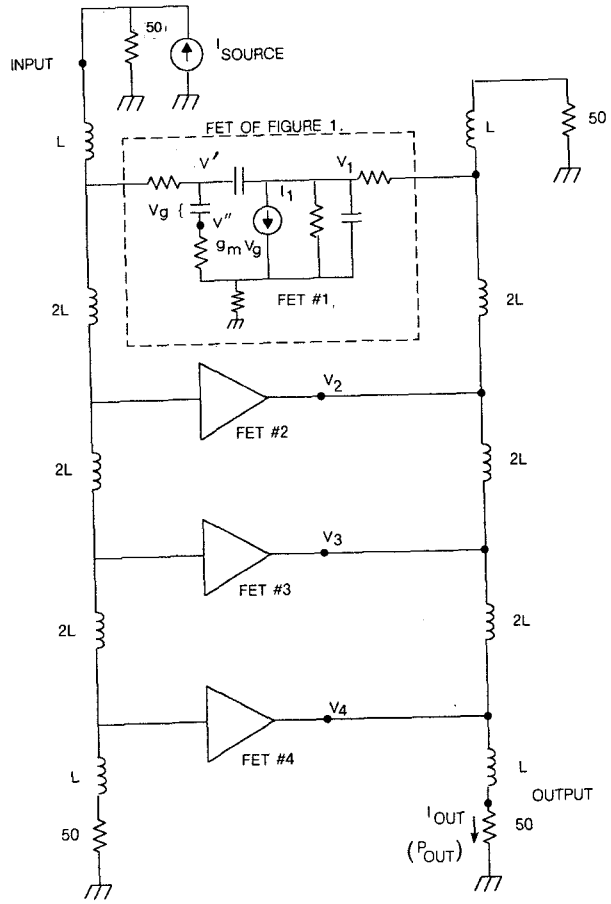

Figure 3. V_1 and I_1 Are the Node-Voltage/Branch-Current Sampling Points for Load-Line Analysis.

the drain line gives too low a load resistance for the unit FET width for each section, and the higher the desired frequency of operation, the smaller the unit FET width and the less optimum the load presented to each FET.

2 X 4 DA

Further load-line analysis shows how the 2 X 4 DA design of reference [1] gives better large-signal performance. By having two gate lines with the individual FET drains driving a common drain line (Figure 5), an effective higher impedance load line results for each FET. Figure 6 shows the load line of each of the four FET pairs (1a & 1b of Figure 5 are combined, for example), and as a group the load lines generally fill the area of the I-V characteristics in a more optimum fashion.

ELECTRONIC LOAD OF A MULTI-FET CIRCUIT

In the case of a distributed amplifier all the FETs are driven simultaneously in order to have a valid simulation of the load each FET

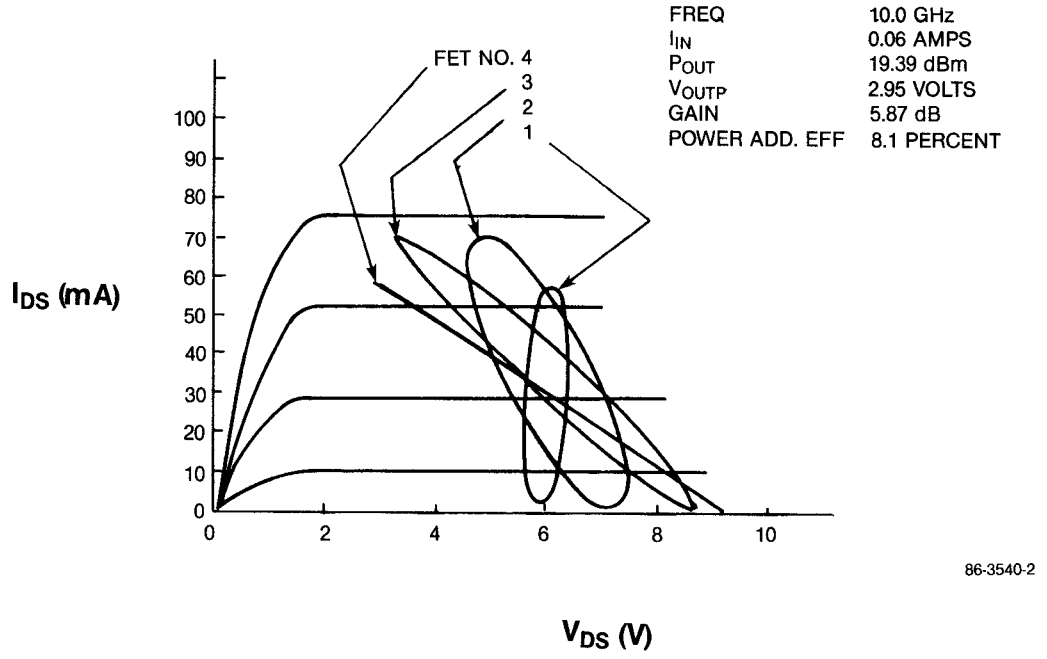

Figure 4. Load-Line Ellipses for the 4 FETs of Figure 3 for a 1 X 4 Conventional DA. Individual FET gate width is 200 microns.

sees. The voltage on the drain line affects the impedance each individual FET has to drive. For example, one ampere into a one-ohm resistor has the obvious correspondence of one volt across the one-ohm resistor, but if a second one-amp current source is connected to the one-ohm resistor there results two volts across the resistor with the result that each current source drives a two-ohm load, the electronic load being different than the circuit element value [2]. The voltage along the drain line of the distributed amplifier complicates the assessment of the load impedance each device sees but which load-line analysis makes readily apparent.

EXPERIMENTAL RESULTS

A 2 X 4 amplifier was designed and fabricated using this approach. The chip is shown in Figure 7 with two gate lines (top and bottom) and one drain line (middle). The chip was designed to work from 6-18 GHz with 0.25 W output power. Flat gain and power were measured across the entire band as shown in Figure 8. The power output was predicted from load-line analysis similar to the examples of Figures 5 and 6 and agreed to within 0.5 dB of the measured power characteristics of Figure 8. Furthermore, during the design, consideration was given to having the FETs go into saturation uniformly across the band, and the load-line analysis gave the necessary design feedback to make the uniform compression possible. A SPICE analysis for several frequencies, for four FET pairs, and for several power levels would have been too time consuming to be useful to the designer.

CONCLUSION

In summary, load-line analysis has been applied to amplifier design in an area where SPICE analysis has limitations. Design information is readily apparent because the appropriateness of a given load line as being near optimum is readily apparent. Circuit parameters can then be adjusted to bring in the load line for each device to near the optimum. Load lines of several devices at several frequencies can be displayed at once, again allowing the designers to quickly see where the circuit needs correcting. The branch current for each FET is sampled inside the FET model, and calculations have agreed with the measured results within 0.5 dB.

REFERENCES

[1] Y. Ayasli et al., "2-20-GHz GaAs Traveling-Wave Power Amplifier," IEEE Trans. Microwave Theory and Tech., Vol. MTT-32, pp. 290-295, Mar. 1984.

[2] Gilson, R.A. Private discussion of load seen by one FET in a multi-FET circuit.

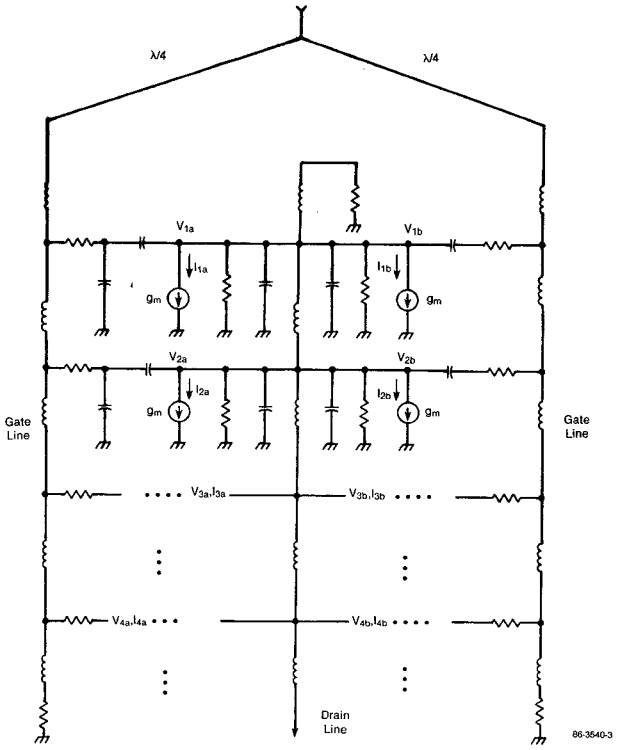

Figure 5. 2 X 4 Distributed Amplifier [1]; i.e., Two Gate Lines and One Drain Line.

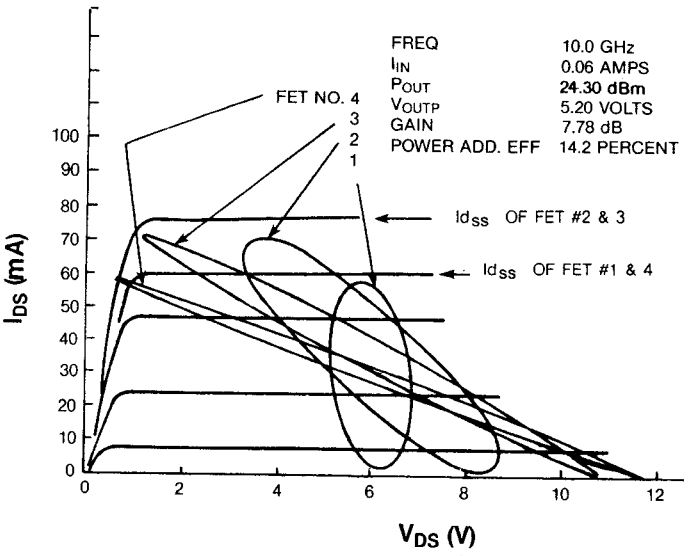

Figure 6. Load-Line Ellipses for the 2 X 4 DA of Figure 5 Show Near Optimum Load Lines for 3 Out of 4 FETs.

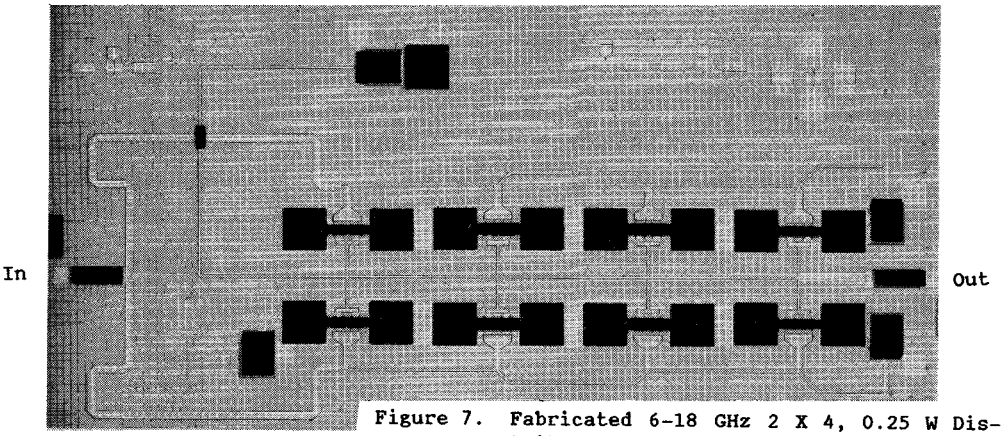

Figure 7. Fabricated 6-18 GHz 2 X 4, 0.25 W Distributed Amplifier.

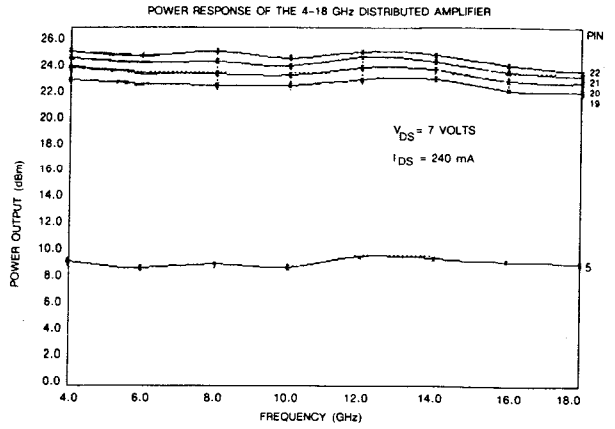

Figure 8. Measured Performance of 2 X 4 Distributed Amplifier of Figure 7.